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FELLERS SNIDER BLANKENSHIP
BAILEY & TIPPENS
THE KENNEDY BUILDING
321 SOUTH BOSTON SUITE 800
TULSA, OK 74103-3318

EXAMINER

STEELMAN, MARY J

ART UNIT

PAPER NUMBER

2191

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/825,098	Applicant(s) FOEGELLE ET AL.	
	Examiner Mary J. Steelman	Art Unit 2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5 and 7 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6 and 8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is in response to amendments and remarks received 25 July 2005. Per Applicant's request, claims 2, 5, and 7 have been amended. Claims 1-8 are pending.

Allowable Subject Matter

2. Claims 5 and 7 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding independent claim 5, as Applicant has pointed out on page 10, 4th paragraph, of Remarks, received 25 July 2005, cited prior arts taken alone or in combination, fail to disclose, "when said translator is in a third operational mode, said primary interface is in electrical communication with said secondary interface such that at least a portion of a serial data message transmitted on said secondary bus is replaced by data stored in said data storage as said serial data message is communicated to said primary one wire bus."

Regarding independent claim 7, as Applicant has pointed out on page 11, last paragraph through page 12, 1st paragraph, of Remarks, cited prior arts taken alone or in combination, fail to disclose,

"(I) if said memory command is a read command performing the steps of:

- (i) at said translator, receiving slave data on said secondary one-wire bus;
- (ii) from said translator, transmitting said slave data on said primary one-wire bus;"

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and

“(m) if said memory command is a write command, performing the steps of:

- (i) at said translator, receiving slave data on said primary one-wire bus;
- (ii) from said translator, transmitting said slave data on said secondary one-wire bus;
- (iii) at said translator receiving verification data on said secondary one-wire bus;
- (iv) from said translator, transmitting said verification data on said primary one-wire bus;
- (v) at said translator, receiving a write pulse on aid primary one-wire bus;
- (vi) from said translator, transmitting a write pulse on said secondary one-wire bus;
- (vii) at said translator, receiving said slave data on said secondary one-wire bus;
- (viii) from said translator, transmitting said slave data on said primary one-wire bus;”

Response to Arguments

3. Applicant has argued, in substance, the following:

(A) Regarding independent claim 1, as applicant has noted on page 9, last sentence of 3rd paragraph, (and similarly argued in reference to claim 8 on page 12, 3rd paragraph), “There is no disclosure of directing data flow between two distinct busses.”

Examiner’s Response: The Curiger reference, FIG. 1 depicts a one-wire processor system. #20 may be considered a primary one-wire bus, #10 may be considered a secondary one-wire bus, #100 may be considered the translator, #300 may be considered the Master, #200 may be considered the Slave. The primary and secondary buses indicate that data flows in both directions. A data direction switch is implied in the translator, as data travels both directions.

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(B) Regarding claim 6, as Applicant has noted on page 11, 2nd paragraph, “none of the cited references discuss interrupting data flowing between two buses to insert known data into the data stream.”

Examiner’s Response:

Claim 6 is very broad. “Sending known serial data” could be any signal supplied in the bus communication. As an example of interrupting data flowing between two buses to insert known data, see col. 6, lines 5-30. Known data stored in registers may be transferred to the network master #300. Inherently, the data flow is ‘interrupted’ to insert this data. See rejection of claim 6 below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-4, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,862,354 to Curiger et al.

Per claim 1:

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-a primary one-wire bus, said primary one-wire bus in digital electrical communication with the master;

(Curiger: Col. 2, lines 15-17, "The present invention is a processor system that incorporates a UART adapted to operate on a one-wire bus. The UART can be master or slave device on the one-wire bus." See FIG. 1, #20 implies a primary one wire bus, #300 implies a master, the drawing shows the primary one wire bus in communication with the master.)

-a secondary one-wire bus, said secondary one-wire bus in digital electronic communication with the one or more slave devices;

(Cruiger: See FIG. 1: #10 implies a secondary one wire bus, #200 implies a slave device. The drawing shows the secondary one wire bus in communication with the slave.)

-a data direction switch for directing the flow of data between said primary one-wire bus and said secondary one-wire bus.

(Curiger: See FIG. 1: #100 implies a translator which inherently provides a data direction switch, as the drawing shows data traveling in both directions, into and out of the translator to the master or the slave. Additionally Curiger disclosed data direction between a master device and multiple slave devices over a one-wire bus, using a status register. Col. 2, lines 56-57, "...can communicate in a bi-directional manner via an exemplary one-wire UART over a one-wire data bus.", col. 6, lines 16-17, "...status register indicates that microprocessor is to receive data from the network master..." (status register is used to indicate which direction data is to

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flow), col. 6, lines 9-11, "...status register...indicating that the microprocessor wants to send data...", col. 6, lines 20-27, "...network master periodically interrogates status registers...to determine which slave UARTS have data to be transferred...")

Curiger disclosed (Abstract, lines 1-9), "...system is adapted to communicate over at least one one-wire network utilizing one-wire communications protocol...For the embodiment of the invention in which the processor communicates over two one-wire networks..." Thus Curiger suggested a plurality of one wire communication buses. Curiger disclosed (col. 2, lines 64-67, "it is understood that if more than one master one-wire UART is incorporated into the same integrated circuit that each should preferably communicate (direct flow of data) on separate one-wire networks (a suggestion of two one-wire buses). While Curiger did show data traveling in both directions, Curiger failed to explicitly disclose a primary and a secondary one-wire bus with a data direction switch for directing the flow.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Curiger by including specific details as suggested by FIG. 1, regarding bi-directional data, which inherently requires a switch for directing a flow.

Per claim 2:

-said secondary one-wire bus is a first secondary one-wire bus and the translator further comprises a second secondary one-wire bus.

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(Curiger: Col. 2, lines 64-67, "...if more than one master one-wire UART is incorporated into the same integrated circuit that each should preferably communicate (translator used to communicate) on separate one-wire networks. (primary and secondary one-wire buses)", col. 4, lines 55-56, "...wherein each one-wire UART is connected to a separate one-wire network..."

Two or more one-wire buses can exist. The translator, directing the flow of data, bridging between a primary and secondary one-wire bus, may itself be a one wire device. Col. 2, lines 16-17, "The UART can be a master or slave device on the one-wire bus." In this case, a translator, controlling data flow between two one-wire buses, becomes a master device, initiating commands. Col. 3, lines 7-8, "A slave UART replies based on what it is told to do via a one-wire network master circuit (translator).")

Per claim 3:

-a command parser for decoding a plurality of commands from the master.

(Curiger: Col. 3, lines 13-14, "A master UART is the controller, hence master, of its one-wire bus. The master UART is responsible for querying the slave circuits connected to the one-wire bus", col. 3, line 45, "...master UART initiates and controls communications...", col. 4, lines 18-25, "...in the embodiment where CPU uses software and a standard port pin to emulate a master UART, the CPU must perform all of the tasks normally performed by a UART, which includes setting up appropriate bit patterns for handshaking purposes, transmitting the appropriate signals...waiting...and reading the responses...(parser decodes for a read)")

Per claim 4:

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-data memory wherein data stored in said memory is output on said primary bus in response to at least one command of said plurality of commands.

(Curiger: Col. 4, lines 9-11, "CPU may perform all of the processing necessary for transmitting data out of a port", col. 7, lines 21-23, "The one-wire UART of the present invention enables a microprocessor to communicate (output data) to other circuits via a one-wire bus.")

Per claim 6:

A method (col. 2, lines 49-50) for inserting known data into a serial data stream between a master and a slave device on a one-wire bus including the steps of:

(a) providing a translator having a primary one-wire bus in electrical communication with the master and a secondary one-wire bus in electrical communication with the slave device, said translator providing interruptible communication between the master and the slave device;

(Curiger: See FIG. 1, #100 acts as a translator providing interruptible communication between a master and slave device. #300 may be the master device, #200 may be the slave device.

(b) decoding a set of commands sent by the master on the primary one-wire bus;

(Curiger: As an example of decoding commands sent by the master see col. 6, lines 12-19, where a read command sent by the network master #300 is decoded and handled by slave devices.

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(c) in response to one or more commands of said set of command, interrupting communication between the master and the slave device;

(Curiger: As an example (col. 6, lines 5-10) data in the status registers (#140(2) and data register (#150(1)) may be provide data to be sent to the network master to indicate that the microprocessor #400 wants to send data. Inherently, communication is interrupted to send this intention.

(d) sending known serial data to either the master or the slave device.

(Curiger: As an example, (col. 6, lines 20-30) known serial data is kept in the registers is transferred (sending) to the network master #300.)

Curiger disclosed a device FIG. 1, #100, that acts as a translator between one-wire buses (#10 & #20). Curiger failed to explicitly disclose 'decoding'. However, it is inherent that a command that is sent to initiate a data transfer from a data register set includes 'decoding' the message sent.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Curiger to explicitly include details regarding serial buses, and communication commands sent and decoded to direct a transfer of known register data.

Per claim 8:

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A translator device for insertion between a master and one or more slave devices on a one-wire bus, thus dividing the won-wire bus into two one-wire buses, the translator device comprising:

- data memory;

- a primary one-wire bus, said primary one-wire bus in digital electrical communication with the master;

- a secondary one-wire bus, said secondary one-wire bus in digital electronic communication with the one or more slave devices;

- data direction switch for alternatively directing the flow of data between said primary one-wire bus and said secondary one-wire bus or between said primary one-wire bus and said data memory.

See rejection of limitations as addressed in claim 1 above.

Conclusion

6. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached at (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman



10/132005


WEI Y. ZHEN
PRIMARY EXAMINER